2.6

Student Performance and Learning Outcome

2.6.1 Programme and course outcomes for all Programmes offered by the institution are stated and displayed on website

Supporting Document : Sample Course File

PCC - 4

Regent Education & Research Foundation

Department of Computer Science & Engineering

Course File

Course Name and Code	: Computer Organization/PCCCS302
Name of the Faculty	: Pragati Ghosh
Name of the Program	: B.Tech in Computer Science & Engineering
Year and Semester	: 2nd Year / 3rd Semester
Academic Year and Semester	: 2022-23 / Odd Semester

Prepared By,

Faculty Name	: Pragati Ghosh
Designation	: Assistant Professor

HOD

Department of Computer Science and Engineering
Regent Education & Research Foundation
Barrackpore, Kolkata - 700 121
College Code - 263

HOD, Dept. of CSE

REGENT EDUCATION AND RESEARCH FOUNDATION GROUP OF INSTITUTIONS
PRINCIPAL
BARRACKPORE

Check List of Main Course File

SL NO	Description	Status
1.	University Syllabus (Part A)	
2.	Module Wise Lesson Plan (Part B)	
3.	Assignment, Question Papers of Assessment (Part C)	
4.	Question Paper in Institute Format along with minimum 3 solved Copies *(To be kept separately in General Annexure)*	
5.	Mapping Question with COs	
6.	Question Bank *(To be kept separately in General Annexure)*	
7.	Tutorial Topics & Questions *(To be kept separately in General Annexure)*	
8.	Course Material / Lecture Notes *(To be kept separately in General Annexure)*	

University Syllabus (Part A)

Course Name : Computer Organization

Course Code : PCC-CS302

Credit Points : 3

Prerequisites:

- Concept of basic components of a digital computer, Basic concept of Fundamentals & Program structures. Boolean algebra.
- Basic number systems, Binary numbers, representation of signed and unsigned numbers, Binary Arithmetic as covered in Basic Computation & Principles of Computer Programming.
- Boolean algebra.

Objectives:

1. To prepare students to perform the analysis and design of various digital electronic circuits.
2. To know how Computer Systems work & its basic principles
3. To know how I/O devices are being accessed and its principles etc.

Course Content:

Unit	Content	Hrs. / Unit
1.	Basic organization of the stored program computer and operation sequence for execution of a program. Role of operating systems and compiler/assembler. Fetch, decode and execute cycle, Concept of operator, operand, registers and storage, Instruction format. Instruction sets and addressing modes. Commonly used number systems. Fixed and floating point representation of numbers.	8
2.	Overflow and underflow. Design of adders - ripple carry and carry look-ahead principles. Design of ALU. Fixed point multiplication -Booth's algorithm. Fixed point division - Restoring and non-restoring algorithms. Floating point - IEEE 754 standard.	8
3.	Memory unit design with special emphasis on implementation of CPU-memory interfacing. Memory organization, static and dynamic memory, memory hierarchy, associative memory. Cache memory, Virtual memory. Data path design for read/write access.	10

4.	Design of control unit - hardwired and micro-programmed control. and Token Bucket algorithm. Introduction to instruction pipelining. Introduction to RISC architectures. RISC vs CISC architectures. I/O operations - Concept of handshaking, Polled I/O, interrupt and DMA.	10

Learning Resources

Text Books:

1. Mano, M.M., "Computer System Architecture", PHI.
2. T.K.Ghosh, "Computer Organization and Architecture", McGraw Hill.
3. Hayes J. P., "Computer Architecture & Organisation", McGraw Hill.
4. Hamacher, "Computer Organisation", McGraw Hill.
5. Behrooz Parhami "Computer Architecture", Oxford University Press.

Reference Books:

1. N. senthil Kumar, M. Saravanan, S. Jeevananthan, "Microprocessors and Microcontrollers" OUP
2. Chaudhuri P. Pal, "Computer Organisation & Design", PHI,
3. P N Basu- "Computer Organization & Architecture" , Vikas Pub
4. Rajaraman – "Computer Organization & Architecture", PHI
5. B.Ram – "Computer Organization & Architecture", Newage Publications.

WEB RESOURCES:

1. http://www.indiabix.com/computer-science/organization/
2. http://www.careerride.com/Computerorganization-Interview-Questions.aspx
3. http://www.geeksforgeeks.org/tag/co/

Learning Outcomes/ Course Outcomes:

Upon completion of this module, students will be able to:

Course name	CO	Description
Computer Organization	PCC-CS302.CO1	Illustrate the history of modern computers and the Von Neumann architecture.
	PCC-CS302.CO2	Demonstrate basic number systems, Binary numbers, representation of signed and unsigned numbers, Floating point representation.
	PCC-CS302.CO3	Distinguish the organization of various parts of a systemmemory hierarchy i.e. cache memory , virtual memory etc.
	PCC-CS302.CO4	Understand memory and I/O operations.
	PCC-CS302.CO5	Classify basics of systems topics like, single-cycle (MIPS), multi-cycle (MIPS), parallel, pipelined, superscalar, and RISC/CISC architectures.
	PCC-CS302.CO6	Define different control unit operations and I/O organization.

PO mapping with course outcome and PSO:

Computer Organization Course Outcome mapping to Program Outcome													
CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO2	PSO2
CO1	3	3	3	3	2	-	-	-	-	-	-	-	3	2
CO2	3	3	3	3	3	-	-	-	-	-	1	-	3	2
CO3	3	3	3	1	3	-	-	-	-	-	2	-	1	3
CO4	3	2	3	3	2	-	-	-	-	-	1	-	2	3
CO5	3	2	3	3	-	-	-	-	-	-	2	2	3	3
CO6	3	3	3	2	3	-	-	-	-	-	3	3	3	3
Attainment	3	2.67	3	2.5	2.6	0	0	0	0	0	1.8	2.5	2.5	2.33

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High)

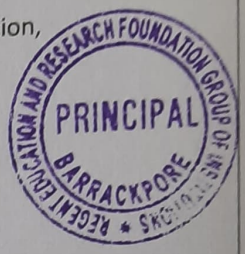
Module Wise Lesson Plan

Sl No.	Topic name	Preferred book	No. Of periods	Cumulative no. Of periods	CO Aimed	Delivery method
	UNIT I					
1	Functional units of a computer and basic operational concepts	T1	1	1	CO1	Chalk & Talk
2	System Design – System representation, Design Process, the gate level	T1	1	2	CO1	Chalk & Talk
3	Register Level – Register level components, programmable logic devices, register level design	T1	1	3	CO1	Chalk & Talk
4	Processor – Level – Processor level components, processor level design	T2	1	4	CO1	Chalk & Talk
5	CPU Organization – Fundamentals, additional features	T2	1	5	CO1	Chalk & Talk
6	Data Representation - Fixed – Point Numbers, Floating Point Numbers	T2	1	6	CO1	Chalk & Talk
7	Addressing modes.	T2	1	7	CO1	Chalk & Talk
8	Instruction Formats, Instruction Types.	T1	1	8	CO1	Chalk & Talk
9	**Tutorial**		1	9		Tutorial
	UNIT II					
10	Fixed Point Arithmetic – Basic adders and subtractors	T2	1	10	CO2	Chalk & Talk
11	High Speed Adders – Carry-lookahead adder, Ripple Carry Adder.	T2	1	11	CO2	Chalk & Talk
12	Multiplication – 2's – complement Multiplier	T2	1	12	CO2	Chalk & Talk

13	Booth's algorithm	T2	1	13	CO2	Chalk & Talk
14	Restoring and Non- Restoring Division algorithm with example	T2	1	14	CO2	Chalk & Talk
15	Modified booth's Algorithm	T2	1	15	CO2	Chalk & Talk
16	Floating Point Arithmetic -Basic Operations, Floating Point Units, Addition Algorithm	T2	1	16	CO2	Chalk & Talk
17	Floating point - IEEE 754 standard- single and double precision.	T2	1	17	CO2	Chalk & Talk
18	**Tutorial**		1	18		Tutorial
	UNIT III					
19	Random Access Memories – Organization, Design	T1	1	19	CO3	Chalk & Talk
20	Serial - Access Memories – Access methods, Organization, Magnetic surface recording	R1	1	20	CO3	Chalk & Talk
21	Multilevel/Hierarchical Memories	T1	1	21	CO3	Chalk & Talk
22	Associative Memory	T1	1	22	CO3	Chalk & Talk
23	Cache Memories – Main features, Organization, Operation	T2	1	23	CO3	Chalk & Talk
24	Cache memory Mapping	T2	1	24	CO3	Chalk & Talk
25	Virtual memory-address translation methods	T2	1	25	CO3	Chalk & Talk
26	Memory Allocation	T2	1	26	CO4	Chalk & Talk
27	Pre-emptive and Non-pre-emptive allocation	T2	1	27	CO4	Chalk & Talk
28	Page Replacement policies	T2	1	28	CO3	Chalk & Talk
29	**Tutorial**		1	29		Tutorial
	UNIT IV					
30	Control Design – Basic Concepts	T1	1	30	CO5	Chalk & Talk
31	Hardwired control – Design Methods	T1	1	31	CO5	Chalk & Talk
32	Micro programmed control-micro instructions, micro program sequencing	T1	1	32	CO5	Chalk & Talk
33	Micro programmed control, CPU Control Unit	T1	1	33	CO5	Chalk & Talk
34	Pipeline Control – Instruction Pipeline	T1	1	34	CO5	Chalk & Talk
35	Communication methods – Basic Concepts, Buses, Bus Control, Interfacing, Arbitration	T1	1	35	CO6	Chalk & Talk
36	IO and system control - IO interface circuits, Handshaking	T1	1	36	CO6	Chalk & Talk

37	DMA – Direct Memory Access	T1	1	37	CO6	Chalk & Talk
38	Interrupts	T1	1	38	CO6	Chalk & Talk
39	Vectored interrupts	T1	1	39	CO6	Chalk & Talk
40	**Tutorial**		1	40		Tutorial

Note:- Delivery method could be chalk & talk, tutorial session, seminar, digital demonstration, assignments



Question Papers of Assessment (Part C)

Assignment-

Question No.	Questions	BL	CO	PO
1	Draw and explain the flow chart for Booth's algorithm	1	1	4
2	Explain 1:16 De-multiplexer with suitable diagram and truth table.	2	2	2
3	Explain the major phases of Instruction cycle.	1	4	2
4	Explain Optimal Page Replacement algorithm for the given string : 3 7 1 7 1 7 3 6 9 1 6 9 3 7 1	1	4	2
5	Write a short note on Half adder and Full Adder.	2	1	2
6	Explain the process of subtraction using two's complement number.	2	1	4
7	Explain the various types of output peripheral devices. State differences between Hardware and Software.	2	2	2
8	Explain CPU Organization.	2	3	4

Internal Assessment-

Answer all the questions given below:

1. How many AND gates are required to design a 16:1 MUX?
   a) 14 b) 15 c) 16 d)17
2. Calculate in binary : (-12 + 9)
   a) 1101 b) 1010 c) 1111 d) 1011
3. 01101 * 01010 = ?
   a) 100110010 b)101000010 c) 110011001 d)100001100
4. DeMUX is used at _____'s end and works as ___.
   a) Sender, Selector b) Sender, Distributor c) Receiver, Selector d) Receiver, Distributor
5. Equivalent hexadecimal of (76575372) will be?
   a) FAFAFF b) FFFAAA c) FAFAFA d) AAFFAF
6. Booth's Algorithm for computer arithmetic is used for ?
   a) Multiplication of numbers in sign magnitude form
   b) Multiplication of numbers in 2's compliment form
   c) Division of numbers in sign magnitude form
   d) Division of numbers in 2's compliment form
7. In IEEE-745 double precision format, exponent = ___ bits.
   a) 11 b) 10 c) 9 d) 8
8. In IEEE-745 single precision format, mantissa = ___ bits.
   a) 52 b) 51 c) 23 d) 24
9. A DEMUX has 6 select lines. What is the no. of input in that DEMUX?
   a) 6 b) 1 c) 64 d) None of these
10. Binary representation of 20.15 is :
    a) 11100.1010011 b) 10001.0010011 c) 10100.1010110 d)10100.0010011
11. In Restoring Division, if Q0 = 0 and Q1 = 1, then the next step will be :-
    a) A=A+M b) A=A-M c) ARS(AQ) d) LS(AQ)
12. A Full Adder can add 2 binary nos. having ___ bits.
    a) 2 b) 3 c) 4 d) 6
13. How many select lines does 128 : 1 MUX has?
    a) 128 b) 64 c) 6 d) 7
14. How many minimum NAND gates are required to make a flipflop?
    a) 2 b) 3 c) 4 d) 5
15. When signed numbers are used in binary arithmetic, then which of the following notation would have unique representation for zero?
    a) Signed magnitude b) 2's complement c) 1's complement d) None of the

Question Paper in Institute Format

GROUP 1	Answer any five questions				(1 * 5 = 5)
Question No.	Questions	Marks	BL	CO	PO
1.a	Find out the 2's complement of the given decimal no.: 14.	1	1	2	4
1.b	Rewrite in descending order – 4 Bits, 4 Terabytes, 4 Nibble, 4 Megabytes, 4 Bytes.	1	1	3	2
1.c	Write +7 in IEEE 32bit format.	1	1	1	2
1.d	How many address bits are required for a 1024* 8 memory?	1	1	1	2
1.e	Find out the Binary of the given Hexadecimal number – A3D2E.	1	1	4	2
1.f	If a memory has 14 page-faults then calculate the Hit and Miss ratio.[Given, total no. of pages = 20.]	1	1	3	2
1g	Which adder is known as n-bit parallel adder?	1	1	3	2

GROUP 2	Answer any four questions				(4 * 5 = 20)
2	Compare Parallel adder with Serial adder. What is the advantage of Carry Look-ahead adder over Ripple Carry adder?	5	4	1	2
3	Suppose, we are given RAM chips each of size 256*4 to design a 4K*16 RAM system. How many smaller chips will be required? Find out the no. of address lines and data lines in the large RAM.	5	1	4	2
4	What is Access Time of a memory? Explain the parameters of a memory.	5	1	2	2
5	Explain Restoring Division using a suitable example.	5	2	3	4
6	Find out the no. of page faults for the given reference string using Optimal Page Replacement algorithm – 2 3 1 3 4 2 1 6 0 7 0 1 2 3 1 1 5 0. [Given, Frame no. = 3]	5	1	3	2
7	What is ALU? Discuss all the units of an ALU.	5	1	1	2